In the Drawings:

Please replace figures 3 and 15 in their entirety with the replacement figures 3 and 15, marked as "REPLACEMENT SHEET", in compliance with 37 C.F.R. 1.84(p)(5) provided herewith.

REMARKS

This preliminary amendment adds no new matter to this application and is supported by the specification. Reconsideration of the application is respectfully requested in light of the following remarks.

Claims 1-41 are pending in the application. In the Final Office Action dated January 6, 2005, the Examiner objected to informalities in the specification and drawings. In addition, Claims 1-5, 8-9, 11-15, 18-19, 22-28, 31, 34-36, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,313,586 to Serge Rutman ("Rutman"). Claims 6-7, 16-17, 29-30, and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of U.S. Patent No. 5,870,109 to Joel C. McCormack et al. ("McCormack et al."). Claims 10, 20, 32, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Betty Prince, "High Performance Memories," 1996 ("Prince"). Finally, claims 21, 33, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman. These rejections are discussed below in connection with the various claims.

I. OBJECTIONS TO THE DRAWINGS FROM THE JANUARY 6, 2005 FINAL OFFICE ACTION

The Examiner objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include reference signs mentioned in the description. The Examiner also objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they include reference signs not mentioned in the description. With this response, replacement drawings complying with 37 C.F.R. 1.84(p)(5) have been provided for figures 3 and 15. Accordingly, Applicants respectfully request these objections of the drawings be withdrawn.

Additionally, the Examiner objected to the drawings for failing to include reference signs 328A and 328B which the Examiner claims are included in the description. With Applicants last response, the specification was amended to remove all instances of reference numerals 328A and 328B. There is no indication in the Final Office Action that this amendment was not entered. In the event that Applicants' previous amendment was not entered, Applicants are resubmitting their previous amendment to paragraph 0074 to remove any mention of reference numerals 328A and 328B. If the amendment was entered, please disregard the currently submitted amendment

to paragraph 0074. In either case, Applicants respectfully request that this objection to the drawings be withdrawn.

II. OBJECTIONS TO THE SPECIFICATION FROM THE JANUARY 6, 2005 FINAL OFFICE ACTION

The Examiner objected to the specification for failing to comply with informalities. In particular, the Examiner noted that the amended abstract included in Applicants' last response failed to conform with 37 C.F.R. §1.121 or 37 C.F.R. §1.72. With this response, Applications have resubmitted their previous amendment to the abstract in accordance with these provisions and respectfully request that this objection be withdrawn.

III. REJECTIONS UNDER 35 U.S.C. § 102(b) FROM THE JANUARY 6, 2005 FINAL OFFICE ACTION

Independent claims 1, 11, 24, and 34 were rejected in the Final Office Action of January 6, 2005 under 35 U.S.C. § 102(b) as being anticipated by Rutman. Applicants submit that claims 1, 11, 24 and 34 are not anticipated by Rutman because Rutman fails to disclose all of the elements of these claims.

Independent claim 1 relates to a "packet processing system." The system includes: "a processor; a co-processor separated from said processor by a boundary; and an interface coupled with said processor and said co-processor and operative to bridge said boundary , said interface including: a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor."

Independent claim 11 relates to an "interface for coupling a processor to a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The

interface includes: "a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor ; and each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor."

Independent claim 24 relates to a "method of interfacing a processor with a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The method includes: "(a) receiving first data from said processor via a first interface; (b) storing said first data in a memory; (c) signaling said co-processor that said first data has been stored; (d) receiving a read command from said co-processor via a second interface; and (e) providing said first data to said co-processor via said second interface across said boundary ; and each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor."

Independent claim 34 relates to an "apparatus for facilitating communications between a first processor and a second processor." The apparatus includes: "a dual port memory coupled with said first processor via first interface and said second processors via a second interface, and operative to act as a message buffer between said first processor and said second processor; control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors of said communications; and each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor ."

Rutman discloses, "A special type of random access memory referred to as video random access memory (VRAM) is used through to provide multiple access to the memory in a timely manner. The VRAM is characterized by a random access port which enables random accessing to the memory array and a serial port comprising a shift register for outputting a large group of

bits of data, such as pixels representative of a scan line of a video image, which are rapidly output by the memory. In the present invention, the VRAM is utilized in a different manner to provide more efficient use of memory without degradation in system performance. The VRAM provides for communications between processors as well as the memory utilized by the coprocessor for storage of code and data. Communications between processors is performed through the serial port; therefore, data is communicated via blocks of data transfers minimizing the frequency of access to the memory array. The co-processor, which utilizes the memory for processing and code storage, communicates with the memory through the random access port in order for the co-processor to perform its functions in a timely manner. The co-processor will only be *interrupted* in its access of the memory when it is determined that blocks of data are to be transferred into the or out of the memory via the serial port." (emphasis added) *See* Rutman, Abstract.

Rutman at least fails to disclose "each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor," as required by claims 1, 11, 24, and 34. The system of Rutman includes a dual ported VRAM having a shift register and a memory array. A main processor utilizes the serial port of the VRAM to write data to the shift register, while a co-processor utilizes the random access port of the VRAM to access the memory array. *See* Rutman, col. 3, ll. 25-65. Rutman specifically discloses that the co-processor will, "*be interrupted in its access of the memory* when it is determined that blocks of data are to be transferred into the or out of the memory via the serial port." *See* Rutman, Abstract (emphasis added). As noted by the Examiner, this results in the co-processor waiting until the following clock cycle to access memory. Applicants respectfully contend that if the access of one device must be interrupted to allow another device to access the memory, this is an access that prevents the other device from accessing the memory. In contrast, Applicants' invention as claimed does not require blocking memory access for one device to enable memory access by another device, but rather provides that the processor and co-processor may access the memory without preventing access to the memory by the other device. For example, a DPSSRAM may be used with control logic to independently driven and isolated the two interfaces of the DPSSRAM by the memory. The network processors may therefore need only contend with making data read and write operations to the DPSSRAM, which makes co-processor operations transparent to the network processors. Application, ¶¶91-

92; see generally, Application, ¶¶91-123. As a result, the processor and co-processor may be able to, for example, store data in the memory at the same time or the processor may store data on one clock edge of a particular clock cycle while the co-processor stores data on the other clock edge of the particular clock cycle. Rutman, in contrast, must interrupt the access of one device to allow that of a second device.

For at least these reasons, claims 1, 11, 24, and 34, as amended, are patentable over Rutman. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

Dependent claims 2-5, 8-9, 12-15, 18-19, 22-23, 25-28, 31, 35-36, and 39 were also rejected under 35 U.S.C. § 102(b) as being anticipated by Rutman. Dependent claims 2-5, 8-9, 12-15, 18-19, 22-23, 25-28, 31, 35-36, and 39 should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

IV. REJECTIONS UNDER 35 U.S.C. § 103(a) FROM THE JANUARY 6, 2005 FINAL OFFICE ACTION

A. REJECTIONS OVER RUTMAN IN VIEW OF MCCORMACK ET AL.

Dependent claims 6-7, 16-17, 29-30, and 37-38 were rejected in the Final Office Action of January 6, 2005 under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of McCormack. Applicants submit that claims 6-7, 16, 17, 29, 30 and 37-38 are patentable over Rutman in view of McCormack because these references, alone or in combination, fail to teach or suggest all of the elements of these claims.

Rutman is described above.

McCormack discloses, "A graphics system for storing and editing graphic images represented by digital data, includes a frame memory for storing pixel data representing graphic images including first and second graphic objects. The pixel data is stored at addresses, each being associated with one or more graphic fragment forming the first and second graphic objects. First and second addresses are respectively associated with those of the graphic fragments forming the first and second graphic objects. A memory controller controls writing and reading the pixel data to and from the frame memory. A fragment editor is provided to receive the pixel data read from the first address and modify the associated fragment with the received pixel data so as to form modified pixel data. An address detector detects the first address responsive to a

request to read the pixel data from the first address and the second address responsive to a subsequent request to read pixel data from the second address. The detector compares the detected first and second addresses to identify an overlap of the first and second graphic objects. If an overlap is identified, the controller controls the writing of the modified pixel data to the first address before the reading of the pixel data from the second address." See McCormack, Abstract.

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor." McCormack et al. fails to fill the gap. McCormack discloses a graphic system which detects overlap between multiple graphic objects to ensure that each frame in the overlap is rendered properly. Nowhere does McCormack et al. disclose or suggest a system "wherein each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor," as claimed.

For at least these reasons, claims 6-7, 16-17, 29-30, and 37-38 are patentable over Rutman in view of McCormack et al. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

B. REJECTIONS OVER RUTMAN IN VIEW OF PRINCE

Claims 10, 20, 32, and 40 were rejected in the Final Office Action of January 6, 2005 under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Prince. Applicants submit that claims 10, 20, 32 and 40 are patentable over Rutman in view of Prince because these references, alone or in combination, fail to teach or suggest all of the elements of these claims.

Rutman is described above.

Prince generally describes the advantages of Synchronous RAM, such as burst synchronous SSRAMs, and includes statistics on the number of cycles required for first through fourth memory accesses.

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor." Prince fails to fill the gap. Prince merely discloses the benefits of using various types of synchronous RAMs. Nowhere does Prince disclose or suggest a system "wherein each

of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor," as claimed.

For at least these reasons, claims 10, 20, 32, and 40 are patentable over Rutman in view of Prince. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

C. REJECTIONS OVER RUTMAN

Claims 21, 33, and 41 were rejected in the Final Office Action of January 6, 2005 under 35 U.S.C. § 103(a) as being unpatentable over Rutman. Applicants submit that claims 21, 33 and 41 are patentable over Rutman because this reference fails to teach or suggest all of the elements of these claims.

Rutman is described above.

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein each of said processor and said co-processor is capable of accessing said memory without preventing access by the other of said processor and co-processor."

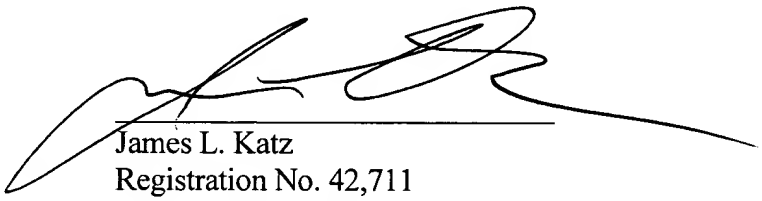
For at least these reasons, claims 21, 33, and 41 are patentable over Rutman. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

SUMMARY

Applicants respectfully submit that all of the pending claims are in condition for allowance and seek early allowance thereof. If for any reason, the Examiner is unable to allow the application in the next Office Action and believes that an interview would be helpful to resolve any remaining issues, he is respectfully invited to contact the attorney of record, James L. Katz, at (312) 321-7739.

Respectfully submitted,

Dated: May 31, 2005



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